AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) In an integrated circuit multiprocessor switching device, an apparatus for mapping a plurality of interrupt sources ~~from~~ and a plurality of ~~data~~ virtual channels to a particular one of a plurality of processors, comprising:

~~a first~~ an interrupt status register for storing ~~at least one interrupt source for a first data channel~~ interrupts;

~~a second interrupt status register for storing at least one interrupt source for a second data channel;~~

mask registers associated with the virtual channels for selectively masking contents of the interrupt status register for each of the virtual channels;

~~an~~ a merged interrupt indication register associated with each ~~data~~ virtual channel for storing ~~a~~ merged and masked interrupt ~~value representing said at least one interrupt source for the associated data channel, where each interrupt indication register is combined to form a merged interrupt status register~~ values for the virtual channels;

an interrupt mapping register associated with each ~~data~~ virtual channel for storing a processor identification for ~~each associated data channel~~ routing masked interrupt value of a respective virtual channel to a selected processor;

~~for each data channel,~~ a demultiplexing circuit coupled to the merged interrupt ~~status~~ indication register and the interrupt mapping register ~~associated with the data channel~~ for coupling the merged and masked interrupt value for ~~the~~ each ~~data~~ virtual channel to ~~a~~ the selected processor ~~identified by the processor identification~~.

2. (currently amended) The apparatus recited in claim 1 formed in a packet manager input circuit for mapping a plurality of interrupts ~~sources from a plurality of input channels such that the first data channel comprises a first input channel and the second data channel comprises a second input channel~~ associated with input of a data packet.

3. (currently amended) The apparatus recited in claim 1 formed in a packet manager output circuit ~~wherein the first data channel comprises a first output virtual channel and the second data channel comprises a second output virtual channel~~ for mapping a plurality of interrupts associated with output of a data packet.

4. (currently amended) The apparatus recited in claim 1 formed in a system controller ~~wherein the plurality of data channels comprises at least one input channel having a first plurality of interrupt sources and at least one output channel having a second plurality of interrupt sources and wherein the merged interrupt status register comprises a first interrupt indication register associated with said at least one input channel for storing a merged interrupt value representing the first plurality of interrupt sources and a second interrupt indication register associated with said at least one output channel for storing a merged interrupt value representing the second plurality of interrupt sources~~ for processing interrupts associated with data packets.

5. (canceled)

6. (currently amended) The apparatus recited in claim ~~5~~ 1 wherein the ~~first mask register is~~ mask registers are programmable to select which interrupts ~~source is~~ are masked.

7. (currently amended) The apparatus recited in claim 1, wherein the selected processor identified by the processor identification determines an interrupting channel by running an interrupt service routine that first reads the merged interrupt ~~status~~ indication register to identify ~~which data channel generated the~~ a virtual channel associated with an interrupt and then reads the interrupt status register ~~corresponding to the identified data channel~~ to determine ~~the~~ a respective interrupt ~~source for the interrupting channel~~.

8. (currently amended) The apparatus recited in claim 1, wherein ~~each~~ the interrupt mapping register further ~~comprises~~ includes a priority level indication associated with each ~~data~~ virtual channel for prioritizing any interrupt issued ~~by the data channel, whereby the demultiplexing circuit selectively couples the merged interrupt value for the~~

~~each data channel to a plurality of prioritized processor interrupt signals under control of the processor identification and priority level indication~~.

9. (currently amended) An interrupt mapper for mapping interrupts ~~from~~ for a plurality of virtual channels to a plurality of processing cores, comprising:

a plurality of ~~source~~ interrupt registers, where each ~~source~~ interrupt register identifies an interrupt ~~sources~~ for one or more of the plurality of virtual channels;

a mask register associated with each of the plurality of ~~source~~ interrupt registers for selectively masking ~~said associated source~~ contents of the interrupt register to generate a masked interrupt ~~sources~~ for each virtual channel;

a channel merge circuit for merging the masked interrupt ~~sources~~ for each virtual channel into an interrupt indication value for ~~said~~ each respective virtual channel;

a channel register that stores the interrupt indication values for the plurality of the virtual channels;

a plurality of processor map storage devices, each processor map storage device storing a processor identification value for respective one of the plurality of virtual channels; and

a demultiplexer coupled to the channel register and the plurality of processor map storage devices for mapping each interrupt indication value for a virtual channel to a selected one of the processing cores identified by the processor identification for that respective virtual channel.

10. (currently amended) The interrupt mapper as recited in claim 9, ~~further comprising~~ wherein the channel merge circuit includes a plurality of AND gates coupled to the ~~source~~ interrupt registers and the mask register[s] for generating the masked interrupt ~~sources~~ for each virtual channel.

11. (currently amended) The interrupt mapper as recited in claim 9, wherein each processor map storage device stores a processor identification value and a priority level for respective one of the plurality of virtual channels.

12. (currently amended) The interrupt mapper as recited in claim 9, wherein the channel merge circuit comprises OR gate circuitry for merging the masked interrupts ~~sources~~ into an interrupt indication value for each virtual channel.

13. (currently amended) The interrupt mapper as recited in claim 9, wherein a processing core that receives an interrupt reads the channel register to determine which virtual channel ~~generated the~~ is associated with an interrupt and then reads the plurality of ~~source~~ interrupt registers to determine a respective interrupt source ~~for the channel's interrupt~~.

14. (currently amended) The interrupt mapper as recited in claim 13, wherein the plurality of ~~source~~ interrupt registers and the channel register are each sized to match a processing width of the processing core.

15. (currently amended) The interrupt mapper as recited in claim 14, wherein the selected processing core determines the source of an interrupt with two register reads.

16. (currently amended) The interrupt mapper as recited in claim 9, wherein ~~interrupts from~~ an interrupt associated with each virtual channel ~~are~~ is mapped to only one processing core.

17. (currently amended) The interrupt mapper as recited in claim 9, wherein the plurality of processor map storage devices are programmable to dynamically assign ~~channel interrupts to the processing cores~~ a processing core to a given virtual channel to implement load balancing among the processing cores.

18-20. (canceled)